REMARKS

This amendment responds to the office action mailed November 22, 2004. In the office action the Examiner:

- objected to claims 11 and 12 for being dependent upon a rejected base claim; and
- rejected claims 1-10 and 13-17 under 35 U.S.C. 103 as being unpatentable over Keeth (US 6,016,282) in view of Toda (US 6,449,727).

After entry of this amendment, the pending claims are: claims 1-17.

Applicants have replaced "read offset value" with "write offset value" in paragraph 0143 of the specification. This amendment is supported by the context surrounding the term in paragraph 0143, which describes an exemplary algorithm of "centering" the write offset value using a minimum amount of time and resources.

The Examiner relies on the text in Keeth at column 8, lines 7 to 42 to support the rejection of claims 1-10 and 13-17. In particular, the Examiner states that this portion of Keeth teaches the first three elements of claim 1. The applicant disagrees. Keeth teaches "sending commands to the first DRAM module 24" and adjusting an adjustment circuit in the DRAM. However, Keeth never says that receiver data is transmitted from the DRAM to the memory controller in this context. This is an important point because the "performing a comparison" element of claim 1 requires comparing the transmitted data sequence from the first element of claim with the receiver data from the third element of claim 1. All that Keeth teaches, during the vernier adjustment process discussed in column 8 of Keeth, is sending commands to the DRAM and adjusting an adjustment circuit in the DRAM.

It is noted that the receiving of data discussed at column 8, line 17 of Keeth concerns receiving write data at the DRAM, not receiving data at the controller.

Furthermore, the sentence of Keeth starting at column 8, line 18, "Next, a read command sequence..." also fails to disclose both the transmittal of a data sequence to a DRAM device and the transmittal of data from the DRAM to the memory controller. In fact, the only sentence of Keeth concerning the read vernier clock adjustment fails to specifically disclose any data transmissions whatsoever. In effect, Keeth teaches the adjustment of an adjusting circuit, but fails to disclose how that result is achieved, other than by sending command sequences to the DRAM.

The only portion of the vernier adjustment discussion in Keeth that discusses both sending and receiving data, is at column 8, lines 35 to 37. However, this portion of Keeth concerns the adjustment of a circuit 60 that is in the memory controller, and circuit 60 is used to adjust the memory controller's sampling time (i.e., for receiving data), and does not concern adjusting the "timing associated with transferring write data" from the memory controller to the DRAM.

Further, Keeth fails to explain how the memory controller is used to adjust the clock adjustment circuit 60 in the memory controller. He simply says that it is done.

In summary, while Keeth fails not only to disclose the comparing element and the generation information based on the comparison element of claim 1, Keeth also fails to disclose transmitting a data sequence to a DRAM and transmitting receiver data from the DRAM to a memory controller in the context of a method for adjusting a timing associated with transferring write data from the memory controller to the DRAM.

Toda, at the locations in column 4 identified by the Examiner, does disclose sending and receiving data, and performing a comparison step. However, Toda's method is for adjusting a clock signal generated within a memory module, not for adjusting a timing for transferring write data from a first integrated circuit, such as a memory controller, to a second integrated circuit, such as a memory module or DRAM device. In addition, Toda fails to teach "generating information representative of a calibrated timing offset" based on a comparison between sent and received data. The controller in Toda never determines or generates any such information. At most, Toda sends the DRAM a signal to increment or decrement a timing offset, without ever generating any "information representative of a calibrated timing offset".

In summary, neither Toda, nor Keeth nor a combination of the two teach or suggest all the limitations of claims 1 and 13, and therefore all the pending claims are patentable over the combined teachings of these references.

In light of the above amendments and remarks, Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-7501 if a telephone call could help resolve any remaining items.

Respectfully submitted,

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(Reg. No.)

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